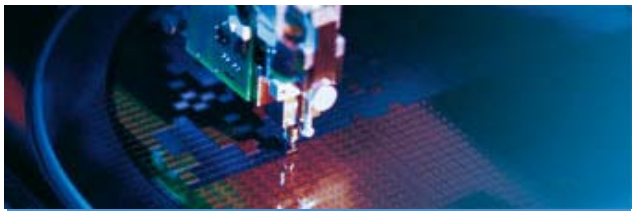
DPD6 USER'S MANUAL



CPU-71-16 (DPD6)

Core i7 VMEbus SBC Module

Second edition – February 2015 – DPD6MAN102

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Preface

Thank you for choosing the CPU-71-16. Please read this manual before using the CPU-71-16 so that you may obtain the greatest benefit from using the device.

This manual presents the specifications, functions, and method of use of the CPU-71-16.

Eurotech has made every effort to carefully inspect each product and has taken great care to package and to ship the product. In the unlikely event of the product's failure to operate normally due to problems in shipping or otherwise, the company will repair or replace the product at its own responsibility.

If you have any questions, contact your local Eurotech Sales Office. See Eurotech Worldwide Presence, page 55 for full contact details.

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VERSION	DATE	Brief Description of Changes	Publication Number
First edition	May 2014 Issued	First Version	DPD6MAN101
Second edition	February 2015 Issued	Vita 31.1 Routing on P0 corrected, IRQ routing for Universe and PMC sites was changed, and GPO2 can reset the VMEbus and the board. Applies to the second rev DPD6.	DPD6MAN102

Table of Contents

1. Important User Information

In order to lower the risk of personal injury, electric shock, fire, or equipment damage, users must observe the following precautions as well as good technical judgment, whenever this product is installed or used.

All reasonable efforts have been made to ensure the accuracy of this document; however, Eurotech assumes no liability resulting from any error/omission in this document or from the use of the information contained herein.

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1.1 Safety Notices and Warnings

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Eurotech assumes no liability for the customer's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Eurotech is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Alerts that can be found throughout this manual

The following alerts are used within this manual and indicate potentially dangerous situations.

Danger, electrical shock hazard:
Information regarding potential electrical shock hazards:
- Personal injury or death could occur. Also damage to the system, connected peripheral devices, or software could occur if the warnings are not carefully followed.
- Appropriate safety precautions should always be used, these should meet the requirements set out for the environment that the equipment will be deployed in.

Warning:
Information regarding potential hazards:
- Personal injury or death could occur. Also damage to the system, connected peripheral devices, or software could occur if the warnings are not carefully followed.
- Appropriate safety precautions should always be used, these should meet the requirements set out for the environment that the equipment will be deployed in.

Information and/or Notes:
These will highlight important features or instructions that should be observed.

Protect the device from vibration and impact

Do not place the product in a location where it can fall or can be subject to vibration or impact because this may cause device failure.

Do not modify the device

For safety reasons, under no circumstances should you modify the device. Eurotech will not repair products that have been modified.

Protect the product from water and chemicals

Contact between the product and water or chemicals can result in product failure, electrocution, or fire.

Protect the product from foreign material

Make sure that foreign material does not get into the product during use, storage, or transport because this can result in product failure.

Use precautions in handling to ensure that you are not injured

The sharp projections on this product may cause injury. Take care in handling this product in order to avoid injury.

Do not disassemble the product

In order to maintain guaranteed product performance, do not disassemble this product under any circumstances.

Keep the product away from radios and TVs

Do not use the product near radios, television sets, or other devices generating strong magnetic or electrical fields. This could result in failure or malfunction.

Keep the product away from flame, humidity, and direct sunlight

Do not use or store the product in any of the following locations, as this could result in product failure:

- Places where there is fire
- Locations high in humidity or exposed to rain
- Locations exposed to direct sunlight
- Dusty or dirty locations
- Locations containing excessive water or chemical vapors

Install the product in well-ventilated locations

Install the product in well-ventilated locations to efficiently disperse heat generated by the product.

Remove the power plug from the receptacle when not using the product

Turn off the main switch and remove the power plug from the receptacle when not using the product or when there is the risk of lightning strike.

Use the device within rated parameters

Be sure to use the product within the ratings specified in this manual. Failure to do so may result in malfunction.

Use care when cleaning the product

If the product becomes dirty, wipe it with a dry soft cloth. A thinned neutral cleaner may be used if the product is particularly dirty. Do not use benzene, thinners, or other solvents under any circumstances.

Ground the product in order to prevent electrocution

Be sure to ground the product by connecting it to a 3-pole AC receptacle or by using an AC receptacle having a grounding terminal.

Dispose of the product properly

Use appropriate methods for handling industrial wastes when disposing of this product.

Wire the product correctly

Failure to wire the product correctly can result in malfunction or fire. Read this manual and wire the product correctly.

Use antistatic precautions

This product comprises electronic parts that are highly susceptible to static electricity. Static electricity can cause the product to malfunction. Take care not to touch any of the terminals, connectors, ICs, or other parts with the hands.

Do not use a malfunctioning product

Stop using the product if you believe it is malfunctioning. Continuing to use a malfunctioning product can cause the malfunction to spread to other products and can cause short circuits or fire.

1.2 Life Support Policy

Eurotech products are not authorized for use as critical components in life support devices or systems without the express written approval of Eurotech.

1.3 Warranty

For warranty terms and conditions users should contact their local Eurotech Sales Office.

See Eurotech Worldwide Presence, page 55 for full contact details.

1.4 RoHS

This device, including all its components, subassemblies and the consumable materials that are an integral part of the product, has been manufactured in compliance with the European directive 2002/95/EC known as the RoHS directive (Restrictions on the use of certain Hazardous Substances). This directive targets the reduction of certain hazardous substances previously used in electrical and electronic equipment (EEE).

1.5 Technical Assistance

If you have any technical questions, cannot isolate a problem with your device, or have any enquiry about repair and returns policies, contact your local Eurotech Technical Support Team. For the CPU-71-16, your first point of contact for technical help should be Dynatem at (949)855-3235 or tech@dynatem.com

See Eurotech Worldwide Presence, page 55 for full contact details.

Transportation

When transporting any module or system, for any reason, it should be packed using anti-static material and placed in a sturdy box with enough packing material to adequately cushion it.

Warning:
Any product returned to Eurotech that is damaged due to inappropriate packaging will not be covered by the warranty.

1.6 Conventions

The following table describes the conventions for signal names used in this document.

Convention	Explanation
GND	Digital ground plane
#	Active low signal
+	Positive signal in differential pair
-	Negative signal in differential pair
NC	No connection
RSVD	Use is reserved to Eurotech

2. Summary

CPU-71-16 is a VMEbus Single Board Computer (SBC) Module based on Intel® Core™ i7 mobile processor. It is compatible with VME64 (ANSI/VITA 1-1994) and VME64x (VITA 1.1-1997) standards which are backwards compatible to the original VMEbus Specification (ANSI/IEEE STD1014-1987).

Based on Hyper-Threading technology, the Intel® Core™ i7 2710UE mobile processor enables simultaneous performance of 4 threads on dual-core, and is suited for applications requiring high performance. Performance in single thread is improved by the Turbo Boost function. It also supports dual displays with its built-in High-performance graphics function. It speeds up encryption and decryption with its built-in AES code engine.

Having direct-mounted DDR3-1333 supporting ECC as the main memory, the CPU-71-16 is suitable for embedded systems requiring high reliability and high performance. Maximum memory capacity is upgradable to 8GB but ships standard OTS with 4GB. The memory automatically corrects 1 bit corruption within 72 bits, and can also detect 2 bit corruption.

The CPU-71-16 was introduced by Dynatem using part number DPD6.

2.1. Features

CPU-71-16 has the following features:

- Intel® Core™ i7 mobile processor
- ECC supported DDR3-1333 memory direct-mounted on board (maximum capacity of memory: 8GB)
- 1 port of 10/100/1000Base-T Ethernet at front panel
- 2 ports of 10/100BaseTX Ethernet on P2 or 2 ports of 10/100/1000BaseTX Ethernet on either P0 or P2 (routing determined by 0 ohm resistors)
- 1 RS232 compatible COM port is available at the front panel via a DB9 connector
- 1 port of Analog SVGA graphics is available at the front panel via a high-density DB15 connector
- 2 ports of USB2.0 interface at front panel
- 1 RS232 COM port routed to the P2 backplane connector
- 3 USB ports are routed to the P2 connector
- 2 SATA ports are routed to the P2 connector
- 1 port of SATA at 3.0 Gb/s interface at optional CFast connector
- 1 port of SATA at 3.0 Gb/s interface at optional P0 VMEbus backplane connector
- The front panel SVGA port may be optionally routed to the P0 connector for use in rugged systems with no front panel I/O
- 1 PMC site with a 32 bit @ 33 MHz PCI (with XMC connector for a x8 PCI Express interface) with I/O accessible from the front panel in standard configuration (PN4 I/O is routed to P0)
- 2nd optional PMC site with 32 bit @ 33 MHz PCI, PN4 I/O is routed to rows d & z of P2
- Universe IID for a VMEbus interface
- Various OSs including Windows 7, VxWorks, and Linux are supported
- RoHS compliant

2.2. Block Diagram

CPU-71-16 Block Diagram is shown in Fig.1.

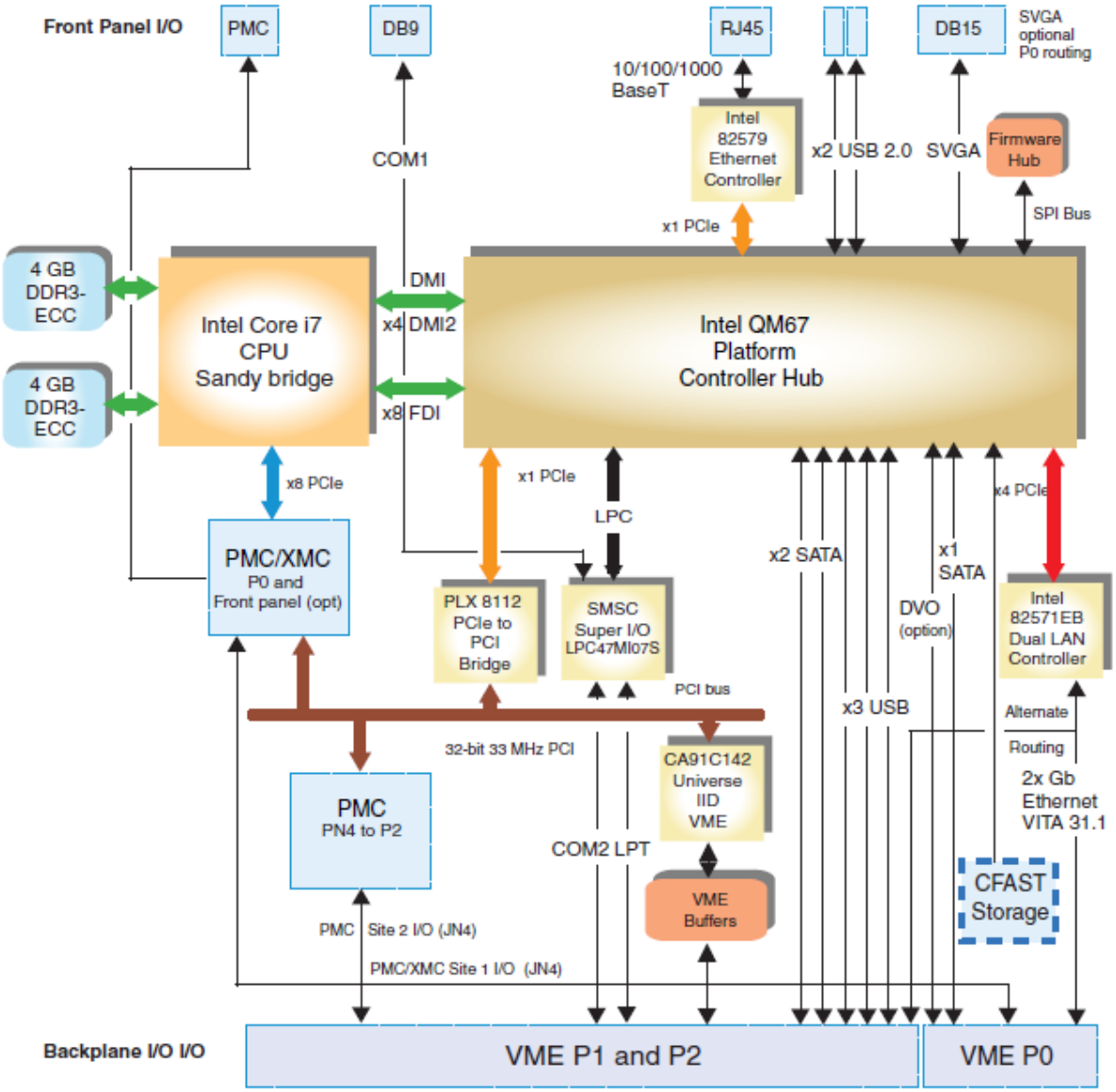


Fig.1 Block Diagram

3. Hardware Specifications

3.1. Processor

3.1.1. Processor Options

- Intel's ®Core™ i7-2610UE Mobile Dual Core CPU at 1.5GHz (TDP:17W) is the off-the-shelf processor, preferable for embedded applications with broader temperature requirements.
- Intel® Core i7-2655LE Mobile Dual Core CPU at 2.2GHz (TDP:25W) is optional.

3.1.2. Cache Memory

CPU-71-16 has the following cache memory:

- L1 cache
  32kB for data, 32kB for instruction (per core)
- L2 cache
  256kB for data and instruction (per core)
- L3 cache (shared by all cores)
  o Core™ i7-2610UE:4MB

3.1.3. I/O Address Map

I/O space Address Map is shown in Table 1.

Table 1. I/O space Address Map

Device	Address
DMA Controller	0000h - 001Fh
Interrupt Controller	0020h - 002Dh
LPC SIO	002Eh - 002Fh
Interrupt Controller	0030h - 003Dh
Timer/Counter	0040h - 0043h
LPC SIO	004Eh - 004Fh
Timer/Counter	0050h - 0053h
Microcontroller	0060h
NMI Controller	0061h
Microcontroller	0062h - 0066h
RTC Controller	0070h - 0077h
DMA Controller	0080h - 0091h
Reset Generator	0092h
DMA Controller	0093h - 009Fh
Interrupt Controller	00A0h - 00B1h
Power Management	00B2h - 00B3h
Interrupt Controller	00B4h - 00BDh
DMA Controller	00C0h - 00DFh
PCI and Master Abort	00F0h
Serial ATA	0170h - 0177h
Serial ATA	01F0h - 01F7h
Serial ATA	0376h
Serial ATA	03F6h
Interrupt Controller	04D0h - 04D1h
Reset Generator	0CF9h

3.1.4. Memory Address Map

Memory space Address Map is shown in Table 2.

Table 2. Memory space Address Map

Device	Address	
Lowest 2 GB of Main Memory	0000_0000h	--- 7FFF_FFFFh
Idt Tsi381 PCI Express - PCI Bridge to the Universe IID VMEbus adapter & the PMC Sites	8000_0000h	--- 9FFF_FFFFh
PCI Express Device	A000_0000h	--- BFFF_FFFFh
Chipset, BIOS, etc	E000_0000h	--- FFFF_FFFFh
Higher 2 GB of DRAM on Cards w/ 4 GB DRAM	1_0000_0000h	--- 1_7FFF_FFFFh
or		or
Higher 6 GB of DRAM on Cards w/ 8 GB DRAM	1_0000_0000h	--- 2_7FFF_FFFFh

.

3.1.5. CPLD Internal Register

CPLD Internal Register is shown in Table 3.

Table 3. CPLD Internal Register map

Register Name	Address	Item
LED Control Register	0000h	3.1.5.1.
Status Register	0001h	3.1.5.2.
Thermal Monitor Select Register	0002h	3.1.5.3.
Thermal Monitor Register	0003h	3.1.5.4.

A CPLD is mounted as internal control logic and for power sequencing. The CPLD's internal register is accessible by the LPC bus of 3.3.8 LPC on page 16. Its base address is 0280h.

The register is configured for 8 bits. Both Read (shown below as: R) and Write (shown below as: W) operations are performed as 8-bit transfers.

R/W : Read and Write
RO : Read only
WO : Write only

3.1.5.1. LED Control Register (offset:0000h)

This register controls LED on CPU-71-16.

Table 4. LED Control Register

bit	Name	Meaning	Initial Value	Access
7..3	RSVD	RSVD	00000	RO
2	LED_EN	1:RED/GRN_LED control enabled 0:RED/GRN_LED control disabled	0	R/W
1	RED_LED	1:LED (RED) On 0:LED (RED) Off	0	R/W
0	GRN_LED	1:LED (GRN) On 0:LED (GRN) Off	0	R/W

※ LED_EN='0' : RED_LED turns on during assertion of the Platform reset that is output by PCH,while GRN_LED turns on during de-assertion. Please refer to 3.5. LED on page 18 for further details.

3.1.5.2. Status Register (offset:0001h)

This register shows the logic of SPD Write Protect signal and input signal from carrier board.

Table 5. Status Register

bit	Name	Meaning	Initial Value	Access
7..4	RSVD	RSVD	000000	RO
3	BIOS_DISABLE#	Request signal from carrier board	-	RO
2	THRM#	1:Temperature sensor on carrier board shows a normal value 0:Temperature sensor on carrier board is shows an abnormal value	-	RO
1	BATLOW#	1:battery voltage on carrier board is a normal value 0:battery voltage on carrier board is an abnormal value	-	RO
0	SPD_WP	WP of EEPROM for SPD Write 0 when rewriting software	1	R/W

3.1.5.3. Thermal Monitor Select Register (offset:0002h)

This register selects a thermal monitor connected to the CPLD that is being read out.

Table 6. Thermal status register

bit	Name	Meaning	Initial Value	Access
7..2	RSVD	RSVD	000000	RO
1..0	THRM_MONI_SEL	Thermal monitor temperature selected from the following options can be read out by thermal monitor register (offset:0003h). 11:RSVD 10:GBE_THRM (ambient temperature of GbE(82579)) 01:DDR3B_THRM (ambient temperature of DDR3(solder side)) 00:DDR3A_THRM (ambient temperature of DDR3 (component side))	00	R/W

3.1.5.4. Thermal Monitor Register (offset:0003h)

This register displays temperature value read out by the thermal monitor.

Table 7. Thermal Monitor Register

bit	Name	Meaning	Initial Value	Access
7..0	THRM	Displays the temperature value read out from the thermal monitor selected by THRM_MONI_SEL (0 to 255℃, 1℃/LSB)	00000000	RO

3.2. Memory

CPU-71-16 memory is shown below.

3.2.1. Main Memory

The main memory of CPU-71-16 is DDR3-1333 SDRAM. 4 GB capacity comes standard off-the-shelf but optional versions with 1GB, 2GB, or 8GB can be specially ordered.

It supports ECC, automatically corrects 1-bit error, and also detects 2-bit errors.

3.2.2. Boot ROM

This is a SPI-FLASH memory directly-mounted on CPU-71-16 with 8MB of capacity.
It stores UEFI (functionally, the “BIOS”) code and configuration data.

3.2.3. External Memory Interface

CPU-71-16 has the following 2 external memory interfaces for mass storage devices and boot options:

- Serial ATA. CPU-71-16 has two 6 Gb/s SATA ports (SATA0 and SATA1) accessible at the front panel, which can boot from mass storage devices through cable connections. SATA2 is a 3 Gb/s port and it is routed to the optional P0 connector to the backplane. SATA3 is also a 3 Gb/s port and it is routed to a CFast connector on-board that facilitates self-contained OS booting.
- USB. CPU-71-16 has 5 USB ports accessible at the front panel, which can boot from USB floppy or USB-CD(DVD)-ROM or a USB flash drive.

3.3. Communication Specifications

CPU-71-16 has the following communication specifications with external devices.

3.3.1. Graphics

The CPU-71-16 has two graphics ports from the QM67 PCH that are accessible from the front panel.

- An SVGA Port with a 340.4 MHz RAMDAC that supports resolutions up to 2048 x 1536 pixels @ 75 Hz. Three 8-bit DACs provide R, G, and B.
- The i7 processor provides 16 PCI Express lanes that may be used for graphics expansion. Eight of these PCI Express lanes remain unrouted but the other 8 have been brought to optional XMC connector, J15. XMC cards cannot be populated on off-the-shelf CPU-71-16 cards as they will mechanically conflict with the front panel connectors.

Table 8. PCI Express Graphics Link Configuration

PCI Express Pin Name	PCI Express Lane	Link Configuration 1	Link Configuration 2	Link Configuration 3
PCIE15	15	X 4	X 8 (unrouted)	X 16
PCIE14	14			
PCIE13	13			
PCIE12	12			
PCIE11	11	X 4		
PCIE10	10			
PCIE9	9			
PCIE8	8			
PCIE7	7	X 8	X 8 (routed to the optional XMC connector J15)	
PCIE6	6			
PCIE5	5			
PCIE4	4			
PCIE3	3			
PCIE2	2			
PCIE1	1			
PCIE0	0			

3.3.2. PCI Express

CPU-71-16 is compliant with PCI Express Rev2.0 standard. The CPU has 16 lanes of PCI Express that were discussed in the previous section. The QM67 PCH offers 8 lanes of PCI Express. Table 9 shows how the 8 PCI Express lanes from the PCH are used and what devices they interface to.

Table 9. PCH PCI Express Configuration

PCH PCI Express lane	Application
PCIE1	Idt Tsi381 PCI Express to PCI Bridge
PCIE2	82579-LM 1 Gbps Front Panel 1 Ethernet Port
PCIE3	Not Used
PCIE4	Not Used
PCIE5	82571EB Dual Ethernet Controller where the ports are routed to the backplane
PCIE6	
PCIE7	
PCIE8	

3.3.3. USB

CPU-71-16 provides two USB 2.0 ports accessible from the front panel via two A type connectors. Three more USB 2.0 ports are routed to the backplane via the P2 connector.

3.3.4. Serial ATA

CPU-71-16 provides 4 ports of Serial ATA in total; two ports (SATA0/1) of Serial ATA 3 (maximum transfer rate: 6Gb/s) that are both routed to the backplane through the P2 connector and two ports (SATA2/3) of Serial ATA 2 (maximum transfer rate: 3Gb/s) routed to an optional P0 backplane connector and a CFast connector, respectively.

3.3.5. Ethernet

CPU-71-16 has an Ethernet port compliant with the 10/100/1000Base-T standard. An 82571EB provides two 10/100Base-T ports routed to the P2 backplane connector or routed to the optional P0 backplane connector (set at the factory at customer's request).

3.3.6. SMBus (System Management Bus)

CPU-71-16 has an I^2C multiplexer at the SMBus interface to carrier board. It also has a SMBus port compliant with the SMBus 2.0 standard. The SMBus address map is shown in Table 10.

Table 10. SMBus Address Map

Device	Address
Main Memory SPD (channel A)	1010 000b
Main memory SPD (channel B)	1010 001b
I^2C multiplexer (PCA9544APW)	1110 000b

I^2C multiplexer channel map is shown in Table 11.

Table 11. I^2C multiplexer channel map

Device	Address
Unused	0
Unused	1
Super I/O	2
Unused	3

Channel is not selected after BIOS start up. Do not switch to channel 0 or channel 3 as they are unused. Please refer to the PCA9544APW (NXP) datasheet for I^2C multiplexer setting method.

3.3.7. PCI

CPU-71-16 has a 32bit/33MHz PCI bus compliant with the PCI Local Bus Specification Revision 2.3 standard. The PCI bus interface is provided by a Idt Tsi381 bridge that adapts from one (x1) PCI Express lane off the QM67 and then is used to interface to the Idt Universe IID PCI bus to VMEbus controller. All VMEbus Interrupts are routed to INTC# on the Tsi381. Additionally, it interfaces to the two optional PMC sites. The signal voltage on the PCI bus is 3.3VDC only.

PCI devices are shown in Table 12.

Table 12. List of PCI devices

Bus number	Device number	Function number	Device	Device model number
0	0	0	DRAM Controller	Intel®Core™ i7/i5
	1	0	PCI Express Controller 1	Intel®Core™ i7/i5
		1	PCI Express Controller 2	Intel®Core™ i7/i5
		2	PCI Express Controller 3	Intel®Core™ i7/i5
	2	0	Integrated Graphics Device	Intel®Core™ i7/i5
	6	0	PCI Express Controller 4	Intel®Core™ i7/i5
	22	0	Intel® Management Engine Interface #1	Intel® QM67
		1	Intel® Management Engine Interface #2	Intel® QM67
		2	IDE-R	Intel® QM67
		3	KT	Intel® QM67
	25	0	Gigabit Ethernet Controller	Intel® QM67
	26	0 to 7	USB EHCI Controller #2	Intel® QM67
	27	0 to 7	Intel® High Definition Audio Controller	Intel® QM67
	28	0	PCI Express Port 1	Intel® QM67
		1	PCI Express Port 2	Intel® QM67
		2	PCI Express Port 3	Intel® QM67
		3	PCI Express Port 4	Intel® QM67
		4	PCI Express Port 5	Intel® QM67
		5	PCI Express Port 6	Intel® QM67
		6	PCI Express Port 7	Intel® QM67
		7	PCI Express Port 8	Intel® QM67
	29	0 to 7	USB EHCI Controller #1	Intel® QM67
	30	0	PCI-to-PCI Bridge	Intel® QM67
	31	0	LPC Controller	Intel® QM67
		2	SATA Controller #1	Intel® QM67
		3	SMBus Controller	Intel® QM67
		5	SATA Controller #2	Intel® QM67
		6	Thermal Subsystem	Intel® QM67
M(*4)	–	–	PCI Express	–

*4 : M depends on the largest bus number shown on PCI Express.

3.3.8. LPC

CPU-71-16 has a port compliant with the LPC1.1 standard. The LPC bus is used for communication with the LPC47M107S-MS Super I/O chip. This device is used by the BIOS and provides one COM port that is accessible from a DB9 connector at the front panel and a 2nd COM port and an LPT1 port that are accessible from the P2 backplane connector.

3.4. I/O

CPU-71-16 has the following interfaces to external devices.

3.4.1. GPIO

CPU-71-16 has a GPI control register and a GPO control register. The features of GPIO are shown below.

3.4.1.1. GPI

CPU-71-16 is equipped with 4 general inputs. They can be read out from the Intel QM67 PCH register. GPI is set as input pin in BIOS. The register where GPI is allocated is shown in Table 13. If the GPI line's jumper is closed, that GPI line will be connected to its corresponding GPO line. For example, if JP5 is shunted (closed), the GPO2 will be routed to GPI2.

Table 13. GPI control register

Signal	Intel QM67connecting pin	Supporting register Bit	Jumper
GPI0	GPIO68	GP_LVL3 bit 4	JP3
GPI1	GPIO69	GP_LVL3 bit 5	JP4
GPI2	GPIO70	GP_LVL3 bit 6	JP5
GPI3	GPIO71	GP_LVL3 bit 7	JP6

High logic level ("1") is read from the register while High level voltage is applied to the input pin, and Low logic level ("0") is read from the register while Low level voltage is applied to the input pin. Please refer to 7.2. Electrical Specifications on page 28 for electrical specifications.

3.4.1.2. GPO

CPU-71-16 is equipped with 4 general outputs. Status can be changed by writing in the Intel QM67 PCH register. GPO is set as the output pin in BIOS. The register where GPO is allocated is shown in Table 14.

Table 14. GPO control register

Signal	Intel QM67connecting pin	Supporting register Bit	Initial setting (logic level)
GPO0	GPIO8	GP_LVL bit 8	High
GPO1	GPIO15	GP_LVL bit 15	Low
GPO2*	GPIO24	GP_LVL bit 24	Low
GPO3	GPIO28	GP_LVL bit 28	Low

It outputs High level voltage when High logic level ("1") is written in the register, while it outputs Low level voltage when Low logic level ("0") is written in it. Please refer to 7.2. Electrical Specifications on page 28 for electrical specifications. The default output levels on these lines are high ("1").

*__Important__: GPO2 is routed to the Universe IID VMEbus interface device and will generate a reset to both the CPU-71-16's CPU and to the VMEbus as well if it is driven low. Dynatem has designed a Watch Dog Timer (WDT) into the power management/sequence CPLD that can use GPO2 to reset the entire system if it times out. Users who are interested in implementing this feature should contact Dynatem for assistance.

3.4.2. Analog VGA

CPU-71-16 has an Analog VGA port, available at front panel connector J26.

3.4.3. Suspend Status

CPU-71-16 routes the SUS_STAT#/SUS_S3#/SUS_S4#/SUS_S5# signals to LEDs. See Section 6.2 for LED locations and descriptions.

4. Mechanical Specifications

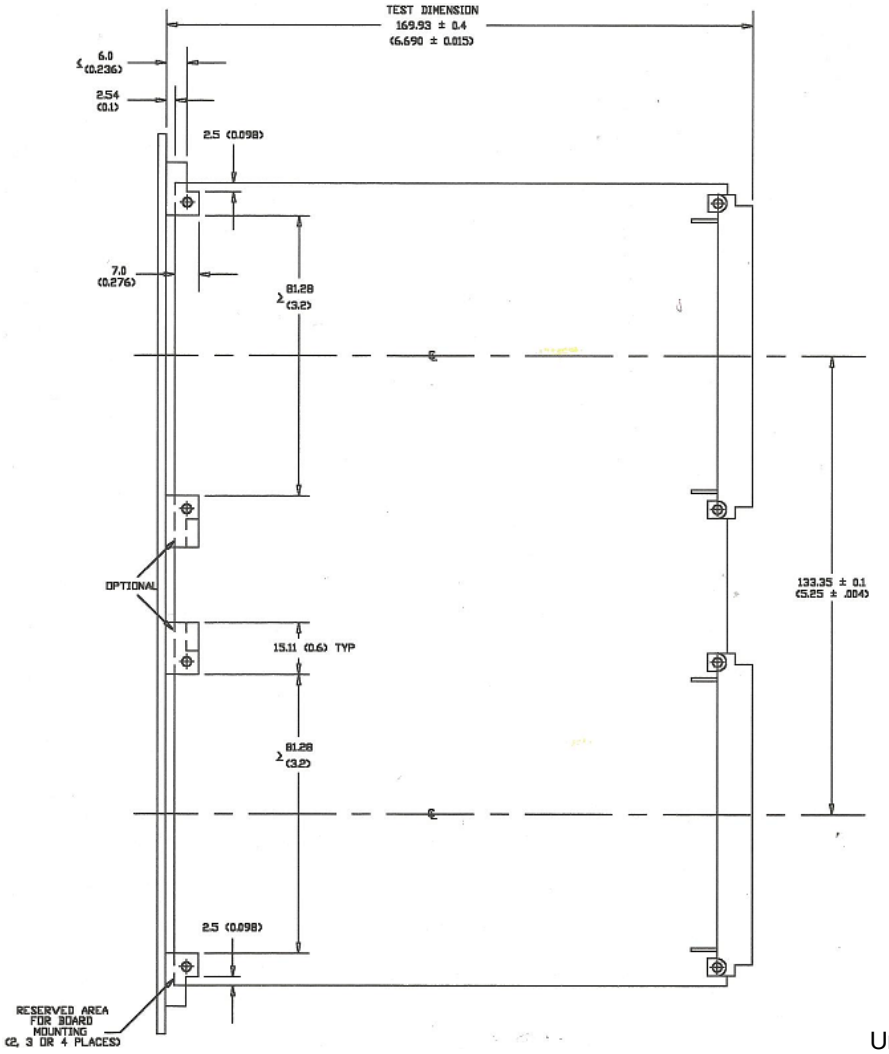
CPU-71-16 is compliant with the VMEbus & VME64 Specification. Mechanical specifications are shown in Table 16.

Table 15. Mechanical Specifications

Characteristic	Contents
PC Board Form Factor	233.35mm high x 153.67mm wide x 2.31mm thick
Backplane Connectors	96 pin DIN 603-2-IEC-CO96Mx-xxx connectors in compliance with the VME64 Draft Specification
Weight	680g (Including heat sink and front panel)

4.1. External Dimension

External dimensions of CPU-71-16 are shown in Fig.2.



Unit : mm (inches)

*5: Height of the mounted components (on the solder side) does not exceed 70 mils..

Fig.2 External dimensions of CPU-71-16

4.2. Front Panel

The DPD6's front panel uses a Rittal Part # 3685-590 Ejector handle.

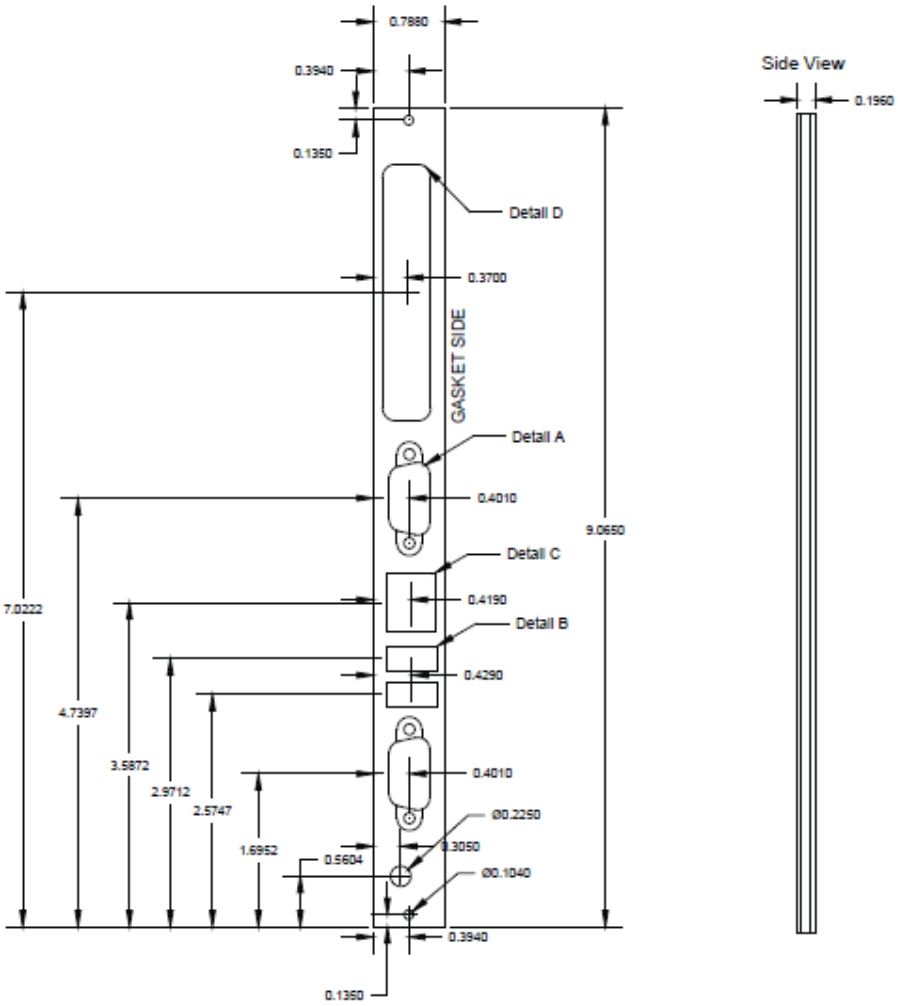


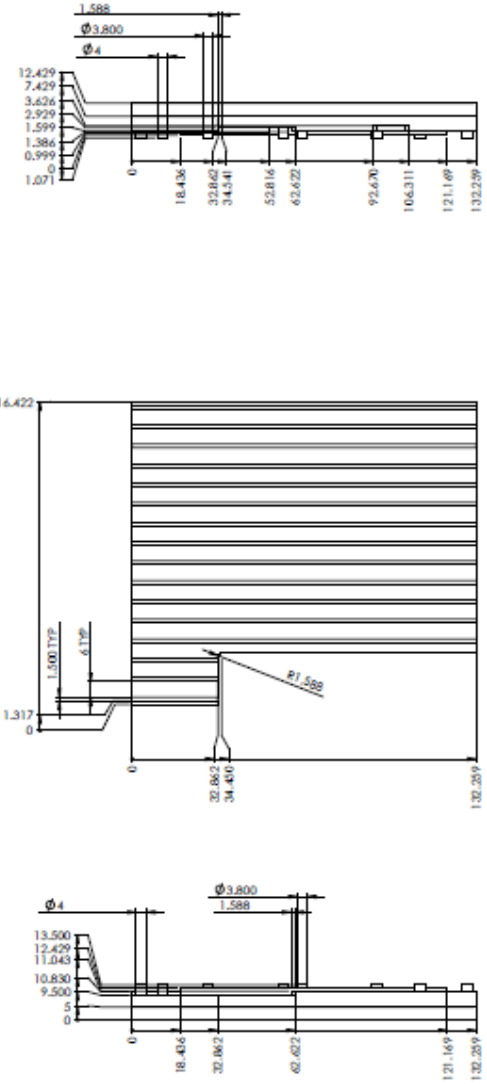
Fig.3. Front panel mechanical drawing

4.3. Heat Sink

The CPU-71-16 comes with a heat sink. The heat sink mainly comes in contact with the CPU, the PCH chipset, and the 82571EB dual Ethernet Controller that routes to the backplane. These are the on-board chips with exposed dies. The fins aid in airflow cooled VMEbus chasses as fans must force air from top to bottom or vice versa. The fins will channel the air and add to the surface area that is exposed to forced air. The units in the mechanical drawing below are in mm.

Table 16. Required heat resistance for cooling system

Processor Type	Heat resistance of cooling system
Intel®Core™ i7-2610UE	Below 2.35℃/W



5. PMC Support and Power Cycling

5.1. Optional PMC

Module Support

5.1.1. General

Versions of the CPU-71-16 that support both PMC sites *must be special ordered* because the 2nd port conflicts mechanically with some front panel connectors. The first site, which also supports a x8 XMC interface, is populated and supported on the CPU-71-16 as standard and there is an opening in the front panel for it. The second PMC site conflicts with the two USB ports, the COM1 port, and the Ethernet port at the front panel.

The Idt Tsi381 chip bridges one PCI Express Rev 2 lane (@ 2.5 Gbps) to the 32 bit @ 33 MHz. The PCI bus is shared between the Universe IID and the two optional PMC sites. The Universe limits the PCI bus's frequency to 33 MHz. Vio is fixed at 5 VDC, again, to be compatible with the Universe IID.

5.1.2. VI/O

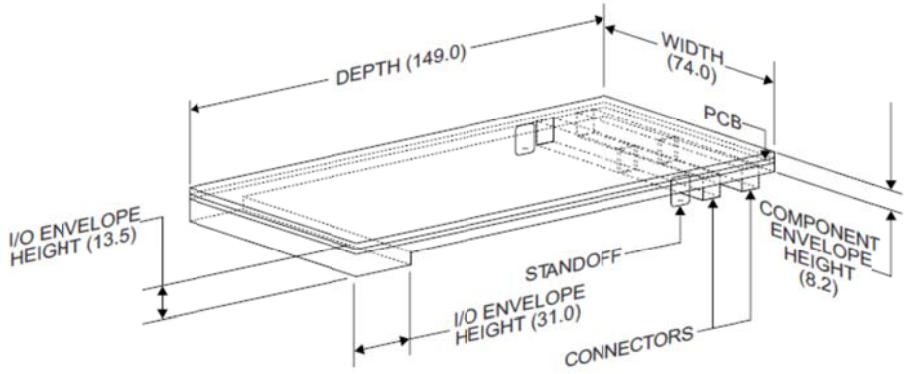
The Tsi381 supports a signalling bus of 5.0 VDC as the PCI bus is shared with the 5 VDC only Universe IID.

5.1.3. JN4 I/O Expansion

The first PMC site's I/O may be routed through the J14 (JN4 PMC functionality) to the optional P0 backplane connector. The second site's I/O may be routed through J24 to the P2 backplane connector.

5.1.4. Mechanical Drawing

The drawing below shows how a PMC card will sit on the CPU-71-16. Space between the PMC card and the CPU-71-16's printed circuit board (PCB) is 0.370".



5.1.5. PMC Interrupts

The PMC sites were designed in compliance with IEEE Standard P1386 Draft 2.3. Please check this specification for the pinout. The first PMC site's interrupts are offset by one so that the board's INTA is routed to INTB on the Tsi381; INTB on the board goes to INTC on the Tsi381 …etc. The 2nd site, in the middle of the board, has its Interrupts offset by two so that INTA on the PMC card will be routed to INTC on the Tsi381…etc.

5.2. Power Sequence

- 12V and 5VDC on the VMEbus have no power sequence but 12 VDC is required to switch on the on-board 5 VDC which is the source for all other voltages.

For internal use:

- Turn the board power off when connecting the SF100 programming tool to the CN1 connector for BIOS reprogramming.

- Do not send the following signals when the CB_RESET# signal is being asserted.

Signals		
LPC_SERIRQ	VGA_I^{2}C_DAT	KBD_A20GATE
SDVO_I^{2}C_DAT	GPI 0 to 3	LPC_DRQ 0 to 1#
LVDS_I^{2}C_DAT	KBD_RST#	LPC_AD 0 to 3

Please make sure that the following signals will have no problem in your design even if voltage is applied from the CPU-71-16 while the carrier board power is OFF.

Signals			
LPC_SERIRQ	SUS_S4#	PCI_FRAME#	LVDS_I^{2}C_CK
LVDS_I^{2}C_DAT	SUS_S5#	PCI_STOP#	LVDS_I^{2}C_DAT
VGA_I^{2}C_DAT	I^{2}C_CK	PCI_IRDY#	VGA_HSYNC
GPI 0 to 3	I^{2}C_DAT	PCI_TRDY#	VGA_VSYNC
KBD_RST#	ATA_ACT#	PCI_SERR#	VGA_I^{2}C_CK
KBD_A20GATE	GPO 0 to 3	PCI_PERR#	VGA_I^{2}C_DAT
LPC_DRQ 0 to 1#	THRMTRIP#	PCI_DEVSEL#	PCI_CLK
CB_RESET#	PCI_GNT0 to 3#	PCI_LOCK#	LPC_CLK
PCI_RESET#	PCI_AD0 to 31	LVDS_BKLT_EN	LPC_FRAME#
SUS_STAT#	PCI_C/BE0 to 3#	LVDS_VDD_EN	LPC_AD0 to 3
SUS_S3#	PCI_PAR	LVDS_BKLT_CTRL	-

If your design does not conform to the above description, please check before using to avoid any problems.

6. Connectors, Jumpers, and LEDs

6.1. CPU-71-16 Placement Plans

A photograph of the CPU-71-16, component side, is shown in Fig.4 with connectors and major components labelled. The solder side is shown in Fig. 5. Fig. 6 labels user option jumpers and LEDs.

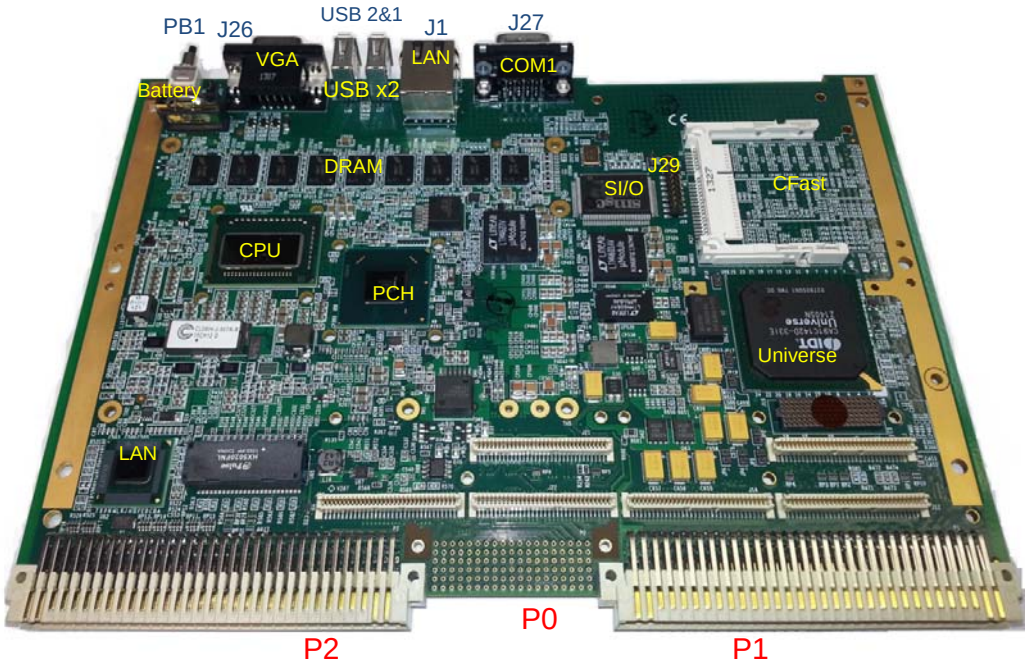


Fig.4 Component side

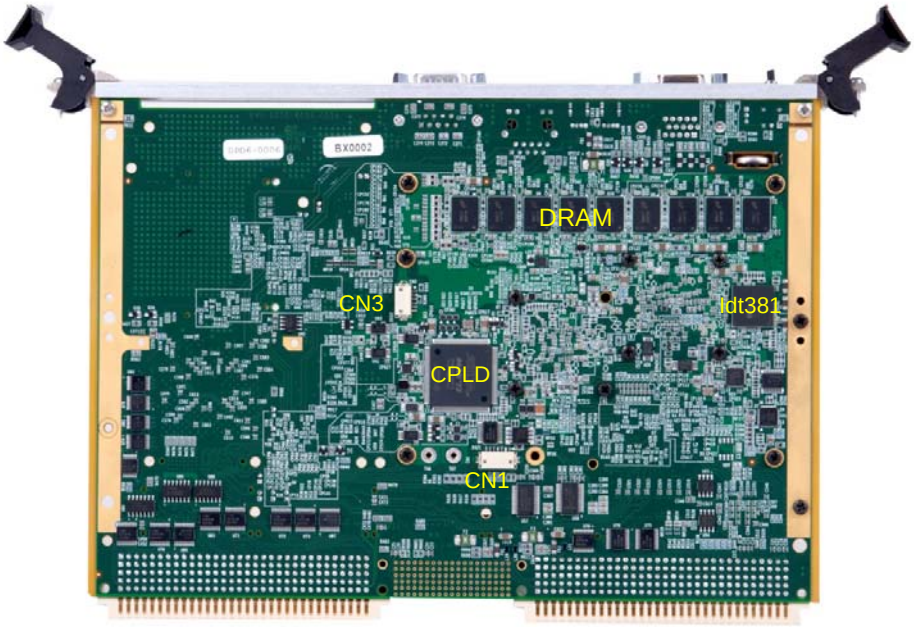


Fig.5 Solder side

6.2. On-board Jumpers and LEDs

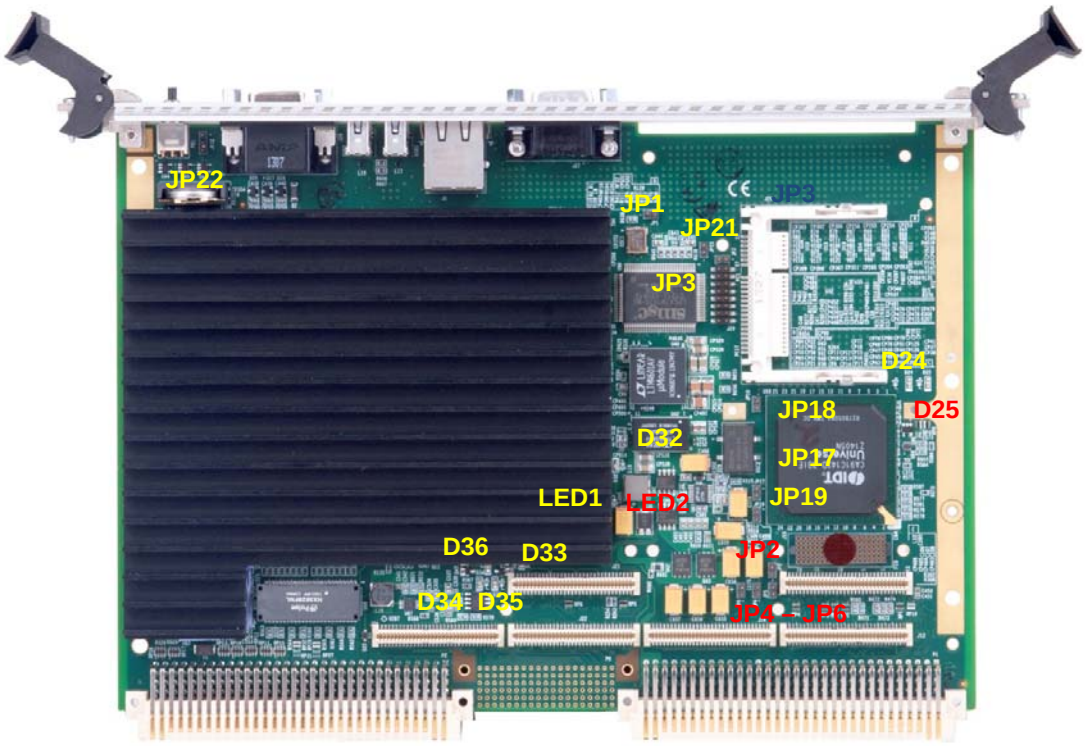


Fig.6 Locations of User Option Jumpers & LEDs

6.2.1. User and Factory Option Jumpers (JPx)

The CPU-71-16 has several user (and factory only) jumpers that are shown in figure 6, above.

Jumper	# of Pins	Description
JP1	2	Clears CMOS and BIOS settings go to default when shunted for 4 seconds while power is off. Jumper JP1 ***must not*** be shunted when power is on.
JP2	2	JP2 will route BATLOW# to Ground when shunted. ***JP2 must be left open.***
JP3	2	JP3 routes GPI0 to GPO0 when shunted.
JP4	2	JP4 routes GPI1 to GPO1 when shunted.
JP5	2	JP5 routes GPI2 to GPO2 when shunted (***Note***: GPO2 will reset the board when asserted low and the VMEbus will also be reset if JP19 is closed).
JP6	2	JP6 routes GPI3 to GPO3 when shunted.
JP17	2	The CPU-71-16 will be hardware initialized to operate as a VMEbus slot 1 bus controller when JP17 is shunted.
JP18	2	The CPU-71-16 will be reset by VMEbus resets when JP18 is shunted and JP22 is shunted between pins 2 & 3.
JP19	2	The VMEbus SYSRESET generated by the Universe IID on the CPU-71-16 will be routed to the VMEbus backplane when JP19 is shunted.
JP21	2	The CPU-71-16 will attempt to boot from an LPC BIOS via connector J29 when JP21 is shunted and this functionality is not supported. ***JP21 must be left open.***
JP22	3	The VMEbus SYSRESET as generated or received by the Universe IID will reset the CPU-71-16's CPU and system resources when JP22 is shunted between pins 2 & 3. Otherwise JP22 must be shunted between pins 1 & 2.

6.2.2. On-board LEDs

The CPU-71-16 has LEDs that provide info on system status and are shown in figure 6, above.

LED	Color	Description
LED1	Green	When LED1 is lit, the on-board power supplies are on and the board should be running.
LED2	Red	When LED2 is lit, the on-board power supplies are in standby mode and the board will not run.
D24	Red	D24 is turned on by pin PC8 (LED1) from the CFast drive at connector J25.
D25	Green	D25 is turned on by pin PC9 (LED2) from the CFast drive at connector J25.
D32	Green	SATA Activity LED from the CPU-71-16 PCH.
D33	Red	Lit when THERMTRIP has been set off, indicating an overheat status.
D34	Red	Lit when the CPU & PCH are in Sleep State S4.
D35	Red	Lit when the CPU & PCH are in Sleep State S5.
D36	Red	Lit when SUS_STAT# has been asserted and the CPU & PCH are entering a sleep state.

6.3. Connector Functionality and Pinouts

6.3.1. CN1 (SPI-ROM programming connector)

CN1 is a connector for writing BIOS data to the on-board SPI-ROM. CN3 will be removed before shipment..

6.3.2. CN3 (CPLD programming connector)

CN3 is a connector for writing data to the on-board CPLD. CN3 will be removed before shipment.

6.3.3. J29 LPC Off-Board Connector

Connector J29 provides off-board LPC routing for alternative BIOS, Super I/O, and also POST code support. This connector is intended for factory use. Here is the pinout for J29:

Odd Row	Signal	Even Row	Signal
1	NC	2	3.3 VDC
3	NC	4	33 MHz Clock.
5	AD0	6	AD3
7	AD1	8	FRAME#
9	AD2	10	GND
11	RESET	12	N/C
13	N/C	14	5 VDC
15	Pullup to 3.3 VDC	16	GND

6.3.4. J1 Front Panel Gigabit Ethernet Port

Connector J1 provides a 1 Gigabit/second Ethernet port accessible at the front panel. There are four differential pairs and they are bidirectional (“BI…”). Here is the pinout for J1:

Pin	Signal
1	BI_DA+
2	BI_DA-
3	BI_DB+
4	BI_DC+
5	BI_DC-
6	BI_DB-
7	BI_DD+
8	BI_DD-

6.3.5. J27 Front Panel RS-232 COM1 Port Connector

Connector J27 provides an RS-232 COM1 port at the front panel. J27 is a male DB9 connector with jack screws for mechanically securing the mating cable connector.

Pin	Signal
1	DCD
2	RxD#
3	TxD#
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RING

6.3.6. J26 Front Panel VGA Connector

J26 is a high-density DB15 VGA connector accessible from the front panel. Here is the pinout for J26:

Pin	Signal
1	Red Output
2	Green Output
3	Blue Output
4	NC
5	HSYNC/VSYNC Return (GND)
6	Red Return (GND)
7	Green Return (GND)
8	Blue Return (GND)
9	+5 VDC
10	HSYNC/VSYNC Return (GND)
11	NC
12	DDCDAT
13	Horizontal Sync (HSYNC) Output
14	Vertical Sync (VSYNC) Output
15	DDCCLK

6.3.7. USB1 & USB2 Front Panel USB Ports

Connectors USB1 & USB2 provide two USB 2.0 ports that are accessible at the front panel. Here is the pinout for either of the two connectors.:

Pin	Signal
1	+5 VDC (via 1.1 amp self-resetting fuse F2)
2	Negative Data
3	Positive Data
4	Signal GND
5	Chassis GND
6	Chassis GND
7	Chassis GND
8	Chassis GND

6.3.8. P1 & P2 & P0 (VMEbus backplane connectors)

P1, P2 are the VMEbus connectors populated on standard off-the-shelf CPU-71-16 cards. They are Harting 160-pin 5-row DIN connectors. Table 17 has the pinout for the P1 connector. P1 is VMEbus spec compliant in its pinout while P2 has custom I/O routing of COM ports, SATA, LAN and LPT1. P1 uses a 5-row connector but the two outside rows (D & Z) are all no connects. The P2 pinout is in Table 18. Outside rows D&Z route the JN4 I/O from optional PMC Site 1 to the backplane as shown.

The optional P0 connector (not populated on the off-the-shelf CPU-71-16) is shown in Table 19. Each pin on row F is connected to Ground. P0 Signals in red font are not in compliance with Vita 31.1.

Table 17. P1 VMEbus connector

RowA		RowB		RowC	
Pin number	Signal	Pin number	Signal	Pin number	Signal
A1	D00	B1	BBSY#	C1	D08
A2	D01	B2	BCLR#	C2	D09
A3	D02	B3	ACFAIL#	C3	D10
A4	D03	B4	BG0IN#	C4	D11
A5	D04	B5	BG0OUT#	C5	D12
A6	D05	B6	BG1IN#	C6	D13
A7	D06	B7	BG1OUT#	C7	D14
A8	D07	B8	BG2IN#	C8	D15
A9	GND	B9	BG2OUT#	C9	GND
A10	SYSCLK	B10	BG3IN#	C10	SYSFAIL#
A11	GND	B11	BG3OUT#	C11	BERR#
A12	DS1#	B12	BR0#	C12	SYSRESET#
A13	DS0#	B13	BR1#	C13	LWORD#
A14	WRITE#	B14	BR2#	C14	AM5
A15	GND	B15	BR3#	C15	A23
A16	DTACK#	B16	AM0	C16	A22
A17	GND	B17	AM1	C17	A21
A18	AS#	B18	AM2	C18	A20
A19	GND	B19	AM3	C19	A19
A20	IACK#	B20	GND	C20	A18
A21	IACKIN#	B21	NC	C21	A17
A22	IACKOUT#	B22	NC	C22	A16
A23	AM4	B23	GND	C23	A15
A24	A07	B24	IRQ7#	C24	A14
A25	A06	B25	IRQ6#	C25	A13
A26	A05	B26	IRQ5#	C26	A12
A27	A04	B27	IRQ4#	C27	A11
A28	A03	B28	IRQ3#	C28	A10
A29	A02	B29	IRQ2#	C29	A09
A30	A01	B30	IRQ1#	C30	A08
A31	-12 VDC	B31	+5 VDC Standby	C31	+12 VDC
A32	+5 VDC	B32	+5 VDC	C32	+5 VDC

Table 18. P2 VMEbus connector

Row A		Row B		Row C		Row D		Row Z	
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	USB_2N	**B1**	+5 VDC	**C1**	COM2 TxD#	D01	P24-1	Z01	P24-2
A2	USB_2P	**B2**	GND	**C2**	COM2 RxD#	D02	P24-3	Z02	GND
A3	USBVBUS0	**B3**	N/C	**C3**	COM2 RTS	D03	P24-4	Z03	P24-5
A4	USB_3N	**B4**	A24	**C4**	COM2 CTS	D04	P24-6	Z04	GND
A5	USB_3P	**B5**	A25	**C5**	COM2 DTR	D05	P24-7	Z05	P24-8
A6	USBVBUS2	**B6**	A26	**C6**	COM2 DSR	D06	P24-9	Z06	GND
A7	USB_4N	**B7**	A27	**C7**	COM2 DCD	D07	P24-10	Z07	P24-11
A8	USB_4P	**B8**	A28	**C8**	COM2 RI	D08	P24-12	Z08	GND
A9	ALT_BAT	**B9**	A29	**C9**	JN4-28	D09	P24-13	Z09	P24-14
A10	LAN2DDP	**B10**	A30	**C10**	Speaker Output	D10	P24-15	Z10	GND
A11	LAN3TDP	**B11**	A31	**C11**	+5 VDC	D11	P24-16	Z11	P24-17
A12	LAN3RDP	**B12**	GND	**C12**	LAN2RDP	D12	P24-18	Z12	GND
A13	LAN3TDN	**B13**	+5 VDC	**C13**	LAN2RDN	D13	P24-19	Z13	P24-20
A14	LAN3RDN	**B14**	D16	**C14**	LAN2CDP	D14	P24-21	Z14	GND
A15	GND	**B15**	D17	**C15**	JN4-30	D15	P24-22	Z15	P24-23
A16	LAN2TDP	**B16**	D18	**C16**	LPT1 STROBE#	D16	P24-24	Z16	GND
A17	LAN2TDN	**B17**	D19	**C17**	LPT1 AUTOFD#	D17	P24-25	Z17	P24-26
A18	LAN2DDN	**B18**	D20	**C18**	LPT1 PD0	D18	P24-27	Z18	GND
A19	LAN2CDN	**B19**	D21	**C19**	LPT1 ERR#	D19	P24-28	Z19	P24-29
A20	GND	**B20**	D22	**C20**	LPT1 PD1	D20	P24-30	Z20	GND
A21	LAN3DDP	**B21**	D23	**C21**	LPT1 INIT#	D21	P24-31	Z21	P24-32
A22	LAN3CDP	**B22**	GND	**C22**	LPT1 PD2	D22	P24-33	Z22	GND
A23	LAN3DDN	**B23**	D24	**C23**	LPT1 SLCTIN#	D23	P24-34	Z23	P24-35
A24	LAN3CDN	**B24**	D25	**C24**	LPT1 PD3	D24	P24-36	Z24	GND
A25	SATA0_TxN	**B25**	D26	**C25**	LPT1 PD4	D25	P24-37	Z25	P24-38
A26	SATA0_TxP	**B26**	D27	**C26**	LPT1 PD6	D26	P24-39	Z26	GND
A27	SATA0_RxN	**B27**	D28	**C27**	LPT1 PD6	D27	P24-40	Z27	P24-41
A28	SATA0_RxP	**B28**	D29	**C28**	LPT1 PD7	D28	P24-42	Z28	GND
A29	SATA1_TxN	**B29**	D30	**C29**	LPT1 ACK#	D29	P24-43	Z29	P24-44
A30	SATA1_TxP	**B30**	D31	**C30**	LPT1 BUSY	D30	P24-45	Z30	GND
A31	SATA1_RxN	**B31**	GND	**C31**	LPT1 PE	D31	GND	Z31	P24-46
A32	SATA1_RxP	**B32**	+5 VDC	**C32**	LPT1 SLCT	D32	+5 VDC	Z32	GND

Table 19. P0 VMEbus connector

Row A		Row B		Row C		Row D		Row E	
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A01	NC	B01	NC	C01	VGA Red	D01	SATA2_TxN	E01	SATA2_TxP
A02	*Opt LPa_DA+*	B02	*Opt LPa_DA-*	C02	GND / VGA Green	D02	LPa_DC+	E02	LPa_DC-
A03	*Opt LPa_DB+*	B03	*Opt LPa_DB-*	C03	GND / VGA Blue	D03	LPa_DD+	E03	LPa_DD-
A04	*Opt LPb_DA+*	B04	*Opt LPb_DA-*	C04	GND / VGA hsync	D04	LPb_DC+	E04	LPb_DC-
A05	*Opt LPb_DB+*	B05	*Opt LPb_DB-*	C05	GND / VGA vsync	D05	LPb_DD+	E05	LPb_DD-
A06	NC	B06	NC	C06	VGA I2C data	D06	SATA2_RxN	E06	SATA2_RxP
A07	PIO5	B07	PIO4	C07	PIO3	D07	PIO2	E07	PIO1
A08	PIO10	B08	PIO9	C08	PIO8	D08	PIO7	E08	PIO6
A09	PIO15	B09	PIO14	C09	PIO13	D09	PIO12	E09	PIO11
A10	PIO20	B10	PIO19	C10	PIO18	D10	PIO17	E10	PIO16
A11	PIO25	B11	PIO24	C11	PIO23	D11	PIO22	E11	PIO21
A12	PIO30	B12	PIO29	C12	PIO28	D12	PIO27	E12	PIO26
A13	PIO35	B13	PIO34	C13	PIO33	D13	PIO32	E13	PIO31
A14	PIO40	B14	PIO39	C14	PIO38	D14	PIO37	E14	PIO36
A15	PIO45	B15	PIO44	C15	PIO43	D15	PIO42	E15	PIO41
A16	PIO50	B16	PIO49	C16	PIO48	D16	PIO47	E16	PIO46
A17	PIO55	B17	PIO54	C17	PIO53	D17	PIO52	E17	PIO51
A18	PIO60	B18	PIO59	C18	PIO58	D18	PIO57	E18	PIO56
A19	VGA I2C clock	B19	PIO64	C19	PIO63	D19	PIO62	E19	PIO61

The Italicized signals on pins A02 – A05 and B02 – B05 were corrected on the second revision of the DPD6 PWB, D010 6097 002A.

7. System Specifications

7.1. Power Supply

Power to the CPU-71-16 is supplied through P1 & P2 (VMEbus backplane connectors), pinout on pages 30 & 31. Power supply specifications are shown in Table 20.

Table 20. Power supply specifications

Item	Symbol	Min	Typ.	Max	Unit
Power supply	VCC_12V	11.4	12	12.6	V
	VCC_5V	4.75	5	5.25	V
	VCC_RTC	2.0	3	3.3	V
Current consumption	I_{VCC_12VDC}	-	-	-	A
	I_{VCC_5VDC}	-	4.1	6.2	A
	I_{VCC_RTC}	-	1.4	-	μA

*8: TDP：under benchmark test with a 45W processor

7.2. Electrical Specifications

7.2.1. GPIO

Electrical specifications of GPIO are shown in Table 21.

Table 21. GPIO electrical specifications

Symbol	Parameter	Min	Typ.	Max	Unit
GPO					
V_{OH}	High level output voltage I_{OH}=-4mA	2.4		3.38	V
V_{OL}	Low level output voltage I_{OL}=4mA			0.45	V
GPI					
V_{IH}	High level input voltage	2.0		3.8	V
V_{IL}	Low level input voltage	-0.5		0.99	V

7.3. Environmental Specifications

Environmental specifications of the CPU-71-16 are shown in Table 22.

Table 22. Environmental specifications

Item	Min	Typ.	Max	Unit
Operating temperature range(*9)	-40		85	℃
Operating humidity range(*10)	35		80	%
Storage temperature range	-40		85	℃
Storage humidity range(*10)			90	%

*9: Cooling system (heat sink, etc.) is necessary for operation
(refer to 4.3. Heat Spreader on page 19)

*10: No condensation

8. BIOS Setup

The CPU-71-16 is equipped with the Phoenix Technologies Ltd. SecureCore Tiano BIOS, customized for this particular board. This chapter describes the BIOS setup procedure. To enter the BIOS setup menus, press the F2 key while immediately after powering up.

Caution:

If the BIOS starting screen or the BIOS setup screen is not displayed properly due to a change in the BIOS settings, clear the CMOS to return to the BIOS default settings by shunting jumper JP1 while power is off (see Section 6.2).

The SecureCore Tiano is a Unified Extensible Firmware Interface (UEFI) and not actually a BIOS but it will be referred to as a "BIOS" in this chapter out of tradition and because their purposes are the same: to initialize the CPU-71-16 and boot the OS. The SecureCore Tiano takes the advantages of a UEFI (faster booting, less limited memory space, greater boot drive size, and support for local I/O devices before booting) and adds a parallel structure that can, as an example, boot the OS while still initializing other devices.

8.1. Main Menu

8.1.1. System Date

Table 1. System Date Menu Setting

Setting	Contents
System Date	Date setting Sets [month: day: year]

8.1.2. System Time

Table 2. System Time Menu Setting

Setting	Contents
System Time	Time setting Sets [hour: minute: second]

8.1.3. System Information

Current system information is displayed.

8.1.4. Boot Features

Table 3. Boot Features Menu Setting

Setting	Contents
NumLock	Set NumLock status at start-up ・On (Default) – ON ・Off - OFF
QuickBoot	Set QuickBoot ・Disabled - disable ・Enabled(Default) - enable
BIOS Level USB	Select USB support to reduce boot time. ・Disabled - disable ・Enabled(Default) - enable
USB Legacy	Select USB SMM support to use mouse, keyboard, mass storage by legacy OS like DOS. ・Disabled - disable ・Enabled(Default) - enable
Console Redirection	Set to use universal console redirection. ・Disabled(Default) - disable ・Enabled - enable
UEFI Boot	Enable UEFI Boot. ・Disabled - disable ・Enabled(Default) - enable
Legacy Boot	Enable Legacy Boot. ・Disabled - disable ・Enabled(Default) - enable
Boot in Legacy Video Mode	Set to boot Legacy Video mode. ・Disabled(Default) - disable ・Enabled - enable
Load OPROM	Select all OPROM load or On Demand load according to Boot device. ・All - All OPROM load ・On Demand(Default) - On Demand load

8.1.5. Error Manager

Setting	Contents
View Error Manager Log	Show Error Log by Enter.
Clear Error Manager Log	Clear Error Log.

8.2. Advanced Menu

8.2.1. Select Language

Table 4. Select Language Setting

Setting	Contents
Select Language	Language can be selected ・English ・Japanese ・French ・Korean ・Chinese

8.2.2. ACPI Configuration

Table 5. ACPI Configuration Setting

Setting	Contents
FACP-RTC S4 Flag Value	Set RTC S4 flag value of FACP table. (Only valid at ACPI) ・Disabled - disable ・Enabled(Default) - enable
APIC-IO APIC Mode	Enable APIC mode. Valid for WindowsXP only ・Disabled - disable ・Enable(Default) - enable
ALS Support	Set ALS support. (Only valid at ACPI) ・Legacy(Default)- ALS support by IGD INT10 ・ACPI - ALS support by ACPI ALS driver
EMA Support	Set to use EMA device in ACPI environment. (Only valid at ACPI) ・Disabled(Default)- disable ・Enabled - enable
MEF Support	Set to support Mobile East Fork in ACPI environment. (Only valid at ACPI) ・Disabled(Default)- disable ・Enabled - enable
Enabled PTID	Enable PTID. ・Disabled(Default)- disable ・Enabled - enable
FACP-PM Timer Flag Value	Set PM timer flag value of FACP table. (Only valid at ACPI) ・Disabled(Default)- disable ・Enabled - enable

8.2.3. Processor Configuration

8.2.3.1. Processor Power Management

Table 6. Processor Configuration Setting

設定	Contents
Active Processor Cores	Set number of cores to be active. ・All (Default)- active all cores ・[Number]-different for each processor core number.
Intel(R) HT Technology	Enable Hyper-Threading technology. When this is disabled, one thread will be active per active core. ・Disabled - disable ・Enabled(Default) - enable
CPU Flex Ratio Override	Set CPU Flex Ratio Override. ・Disabled(Default)- disable ・Enabled - enable
Dynamic FSB Switching	Set processor dynamic FSB switching (BUS GV). ・Disabled - disable ・Enabled(Default) – enable
Enabled XD	Enable Execute Disable which also known as Data Execute Prevention (DEP). ・Disabled - disable ・Enabled(Default) - enable
Enable for BIST	Set execute BIST (Built-In Self Test) at reset time. ・Disabled(Default) - disable ・Enabled - enable
Intel(R) Virtualization Technology	VMM can use virtualization functions. ・Disabled - disable ・Enabled(Default) - enable
Intel(R) Streamer Prefetcher	Enable Stream Prefetcher ・Disabled - disable ・Enabled(Default) - enable
Intel(R) Spatial Prefetcher	Enable Spatial Prefetcher ・Disabled - disable ・Enabled(Default) - enable

8.2.3.2. Processor Power Management

Table 7. Processor Power Management Setting

Setting	Contents
Intel Speed Step (R)	Set processor performance state (P state). ・Disabled - disable ・Enabled(Default) - enable
Boot Performance mode	Set performance mode for boot before handover to OS. ・Max Performance(Default) ・Max Battery ・Auto
Turbo Mode	Enable processor Turbo mode and EMTTM. ・Disabled - disable ・Enabled(Default) - enable
Turbo Mode Power Limit Lock *11	Set Turbo setting lock. TURBO_POWER_LIMIT MSR is locked by enabling, while unlocked by resetting. ・Disabled - disable ・Enabled(Default) - enable
Long Power Limit *11	Set Long Time Limit (Power Limit 1) of Turbo mode by watt. Value setting range is from 0 to fuse value. Setting 0 means fuse value. Cannot set value exceed fuse TDP value. ・Default：0
Long Power Limit Time *11	Set time window (Power Limit 1 Time) of Long Time by second. Value setting range is from 0 to 56. Time window keeping TDP value is displayed. Setting 0 means fuse value. ・Default：28
Short Power Limit *11	Set Short Time Limit (Power Limit 2) of Turbo mode by watt. Value setting range is from 0 to fuse. Setting 0 means fuse value. Cannot set value exceed fuse TDP value. ・Default：0
IA Current Limit *11	Set IA current limit. Value is represented at maximum instantaneous current value, and 1/8 ampere unit. ・Default：896
IGFX Current Limit *11	Set IGFX current limit. Value is represented at maximum instantaneous current value, and 1/8 ampere unit. ・Default：368
Energy Efficient Enable *11	Set CPU Energy Efficient P-States. ・Disabled - disable。 ・Enabled(Default) - enable。
Configure TDP Boot Mode	Select Configure TDP Boot Mode. Skip all cTDP settings by selecting Disable, while dynamic cTDP operates. ・Normal ・Down(Default) ・Up ・Disable

*11: possible to set by changing Turbo Mode to “Enable”

Setting	Contents
Lock TDP setting	Lock of TDP MSR_CONFIG_TDP_CONTROL. ・Disabled(Default) - disable ・Enabled - enable
TDP Custom Setting	Set custom TDP. ・Disabled(Default) - disable ・Enabled - enable
C-States	Enabling standby state (power saving states(C-States)) of processor. ・Disabled - disable ・Enabled(Default) - enable
Extend C-States	Enable P-States change combined with C-States status. ・Disabled - disable ・Enabled(Default) - enable
C3-State *12	Enable Power Saving C3-State of processor. ・Disabled - disable ・Enabled(Default) - enable
C6-State *12	Enable Power Saving C6-State of processor. ・Disabled - disable ・Enabled(Default) - enable
C7-State *12	Enable Power Saving C7-State of processor. ・Disabled - disable ・Enabled(Default) - enable
C7s-State *12	Enable Power Saving C7s-State of processor. BIOS reports C7s instead of C7 by enabling this. ・Disabled(Default) - disable ・Enabled - enable
C7r-State *12	Idling power consumption is reduced by enabling C7r-State. ・Disabled - disable ・Enabled(Default) - enable
C-State Auto Demotion *12	Set about C-State auto demotion. ・Disabled ・C1 ・C3 ・C1 and C3
Cpu C1C3 UnDemotion Enable	Enable processor C1C3 undemotion. ・Disabled - disable ・Enabled(Default) - enable

*12: possible to set by changing Extend C-States to “Enable”

8.2.4. Peripheral Configuration

Table 8. Peripheral Configuration Setting

Setting	Contents
Spread Spectrum Clock	Enable Spread Spectrum Clock. ・Disabled(Default) - disable ・Enabled - enable

8.2.5. HDD Configuration

Table 9. HDD Configuration Setting

Setting	Contents
SATA Device	Set SATA device. ・Disabled - disable ・Enabled(Default) - enable
Interface Combination *13	Set operating mode of SATA controller. ・IDE ・AHCI(Default) ・RAID
Serial ATA port X *13	Show Device ID connected to Port X. When device is not connected, a message “Not Install” is displayed.
Hot Plug *13	Enable hot plug. Note: Hardware support required ・Disabled(Default) - disable ・Enabled – enable
External Port *13	Set port as internal or external. ・Disabled(Default) - disable ・Enabled - enable
Port Topology *13	Set connection mode of SATA 6Gb/s port. Only port 0and port 1 support SATA 6Gb/s. ・DirectConnect ・CableUp(Default)
SATA Device Type *13	Solid State Drive should be selected only when SSD is connected to SATA port. ・Hard Disk Drive (Default) ・Solid State Drive

*13: possible to set by changing SATA Device to “Enable”

8.2.6. Memory Configuration

Table 10. Memory Configuration Setting

Setting	Contents
Memory Frequency Limiter	Select maximum memory frequency (MHz). ・Auto (Default) ・1067 ・1333 ・1600 ・1867 ・2133
Max TOLUD	Maximum value of TOLUD. If "Dynamic" is selected, TOLUD is set automatically based on maximum MMIO of installed graphic controller. ・Dynamic (Default) ・1 GB ・1.25 GB ・1.5 GB ・1.75 GB ・2 GB ・2.25 GB ・2.5 GB ・2.75 GB ・3 GB ・3.25 GB ・3.5 GB
NMode Support	Set NMode support system. ・Auto (Default) ・1 N mode ・2 N mode

8.2.7. System Agent (SA) Configuration

8.2.7.1. DMI Settings

Table 11. DMI Setting

Setting	Contents
DMI Link ASPM Control	Enable SA ASPM (Active State Power Management) of DMI link. ・Disabled (Default) ・L0S ・L1 ・L0S and L1 ・Auto
DMI Gen2 Support Control	Enable SA ASPM (Active State Power Management) of DMI link. ・Disabled (Default) ・Enabled ・Auto

8.2.7.2. Intel (R) VT for Directed I/O (VT-d)

Table 12. Intel (R) VT for Directed I/O(VT-d)Setting

Setting	Contents
Intel (R) VT for Directed I/O(VT-d)	Enable Intel(R) Virtualization Technology (VT-d). ・Disabled (Default) ・Enabled

8.2.7.3. Graphics Configuration

Table 13. Graphics Configuration Setting

Setting	Contents
Internal Graphics	Set internal graphics device. Invalid when external graphics is connected. ・Disabled ・Enabled ・Auto (Default)
Primary Display Selection	Select primary display device. ・IGD ・PEG ・PCI ・Auto (Default) ・Switchable Graphics
GTT Size	Set IGD GTT memory size. ・1MB ・2MB (Default)
Aperture Size	Set graphics aperture size. ・128MB ・256MB (Default) ・512MB
DVMT Pre-Allocated	Select pre-allocated graphic memory size being used internal graphic device. Invalid when external graphics is connected. ・32MB (Default) ・64MB ・128MB

Setting	Contents
DVMT Total Gfx Mem	Set DVMT5.0 DVMT graphic memory size. Invalid when external graphics is connected. ・128MB (Default) ・256MB ・Max
Render Standby	Select IGD Render Standby property. ・Disabled ・Enabled (Default)
IGD Thermal Control	Set IGD thermal control. ・Disabled (Default) ・Enabled
GT Turbo Mode Control	Set GT Turbo Mode control. ・Disabled (Default) ・Enabled
IGD – Boot Type	Select video device activated during POST. Invalid when external graphics is connected. ・VBIOS Default (Default) ・CRT ・EFP ・LFP ・EFP3 ・EFP2 ・LFP2
IGD – LCD Panel Type	Select video device activated during POST. Invalid when external graphics is connected. ・VBIOS Default (Default) ・640x480 LVDS Color Panel ・800x600 LVDS Color Panel ・1024x768 LVDS Color Panel ・1280x1024 LVDS Color Panel ・1400x1050 LVDS Color Panel Reduced Blanking ・1400x1050 LVDS Color Panel ・1600x1200 LVDS Color Panel ・1200x768 LVDS Color Panel ・1600x1050 LVDS Color Panel ・1920x1200 LVDS Color Panel ・Reserved #11 ・Reserved #12 ・Reserved #13 ・Reserved #14 -1280x800 LVDS Color Panel ・Reserved #15 -1280x600 LVDS Color Panel ・Reserved #16
IGD – Panel Scaling	Set IGD – Panel Scaling. ・Auto (Default) ・Force Scaling ・off
IGD – Portable Mode	Set IGD – Portable Mode ・Auto (Default) ・Disabled ・Enabled
Inverter Connection	Selection of inverter connection. ・Internal: inverter from GMCH PWM or GMB (Default) ・External: inverter from PCH

Setting	Contents
GMCH BLC Control	Select GMCH BLC control. ・PWM - Inverted (Default) ・GMBUS - Inverted ・PWM - Normal ・GMBUS - Normal
BIA	Select BIA. When [Auto] is selected, GMCH use VBT default. [Level n] set aggressive level. ・Disabled ・Level 1 ・Level 2 ・Level 3 ・Level 4 ・Level 5 ・Auto (Default)
Spread Spectrum clock chip	Set SSC. ・Off (Default) ・Hardware: SSC is set by chip ・Software: SSC is set by BIOS
IGD – TV Control	Set IGD - TV. Invalid when external graphics is connected. ・VBIOS Default (Default) ・NTSC_M / ・NTSC_J / ・NTSC_433 / ・PAL_B / ・PAL_G / ・PAL_D / ・PAL_H / ・PAL_I / ・PAL_M / ・PAL_N / ・PAL_K / ・PAL_Nc / ・SECAM_L / ・SECAM_B / ・SECAM_D / ・SECAM_G / ・SECAM_H / ・SECAM_K / ・HDTV_STD_SMPTE_240M_1080i59 ・HDTV_STD_SMPTE_240M_1080i60 ・HDTV_STD_SMPTE_295M_1080i50 ・HDTV_STD_SMPTE_295M_1080p50 ・HDTV_STD_SMPTE_296M_720p50
IGD – TV2 Control	Set IGD - TV2. Invalid when external graphics is connected. ・VBIOS Default (Default) ・NTSC_M/ ・NTSC_J / ・NTSC_433 / ・PAL_B / ・PAL_G / ・PAL_D / ・PAL_H / ・PAL_I / ・PAL_M / ・PAL_N / ・PAL_K / ・PAL_Nc / ・SECAM_L / ・SECAM_B / ・SECAM_D / ・SECAM_G / ・SECAM_H / ・SECAM_K / ・HDTV_STD_SMPTE_240M_1080i59 ・HDTV_STD_SMPTE_240M_1080i60 ・HDTV_STD_SMPTE_295M_1080i50 ・HDTV_STD_SMPTE_295M_1080p50 ・HDTV_STD_SMPTE_296M_720p50
IGD – Active LFP	.Set IGD - Active LFP. ・No LVDS (Default) ・Int-LVDS ・SVDO LVDS ・eDP Port A ・eDP Port D
Panel Color Depth	Set Panel Color Depth. ・18 bit (Default) ・24 bit

8.2.7.4. PEG Port Configuration

Table 14. PEG Port Configuration Setting

Setting	Contents
PEG 0 – Gen X	Set PEG0 B0:D1:F0 link speed. ・Auto (Default) ・Gen1 ・Gen2 ・Gen3
PEG 1 – Gen X	Set PEG1 B0:D1:F1 link speed.
PEG 2 – Gen X	Set PEG2 B0:D1:F2 link speed.
PEG 3 – Gen X	Set PEG3 B0:D6:F0 link speed.
Always Enable PEG	Enable always PEG. ・Disabled (Default) ・Enabled
PEG ASPM	Set PEG ASPM. ・Disabled (Default) ・L0s ・L1 ・L0s and L1 ・Auto
De-emphasis Control	Set PEG De-emphasis value. ・-6 dB (Default) ・-3.5 dB
Gen3 Equalization	Implementation of PEG Gen3 equalization procedure. ・Disabled ・Enabled (Default)
Gen3 Root Port Preset	Set Gen3 Equalization preset value for root port. ・1～11 (Default：8)
Gen3 End Port Preset	Set Gen3 equalization preset value for end port. ・0～10 (Default：7)
PEG Sample Calibrate	Set PEG sample calibrate. ・Disabled ・Enabled ・Auto (Default)
PEG Gen3 Equalization Phase2	Set PEG Gen3 equalization phase2. ・Disabled (Default) ・Enabled

8.2.8. South Bridge Configuration

Table 15. South Bridge Configuration Setting

Setting	Contents
HPET Support	Set HPET (High Precision Event Timer).When enabled, corresponding enable bit will be set by RSDT point HPET table. ・Disabled ・Enabled (Default)
HPET Memory Map BAR	Select HPET memory map BAR address. ・FED00000 (Default) ・FED01000 ・FED02000 ・FED03000
State After G3	Set the state which will be moved when power is back after G3 state. ・State S5 (Default) ・State S0
Native PCI Express	Set Native PCI Express. ・Disabled (Default) ・Enabled

8.2.8.1. SB PCI Express Configuration

Table 16. SB PCI Express Configuration Setting

Setting	Contents
PCI Express Root Port Clock Gating	Set PCI Express Root Port Clock Gating. ・Disabled ・Enabled (Default)
DMI Link ASPM Control	Set DMI link ASPM (Active State Power Management). ・Disabled (Default) ・L0S ・L1 ・L0S or L1 ・Auto
DMI Link Extended Sync Control	Control of DMI link extension synchronous. ・Disabled (Default) ・Enabled
DMI Link Extended Sync Control	Control of DMI link extension synchronous. ・Disabled (Default) ・Enabled
PCIe-USB Glitch W/A	Work Around to abnormal signal of PCIe-USB by fault device connected to the behind of PCIE/PEG port. ・Disabled (Default) ・Enabled
PEG ASPM	Set PEG ASPM. ・Disabled (Default) ・L0s ・L1 ・L0s and L1 ・Auto
De-emphasis Control	Set PEG De-emphasis value. ・-6 dB (Default) ・-3.5 dB

Setting	Contents
Gen3 Equalization	Implementation of PEG Gen3 equalization procedure. ・Disabled ・Enabled (Default)
Gen3 Root Port Preset	Set Gen3 Equalization preset value for root port. ・1～11 (Default：8)
Gen3 End Port Preset	Set Gen3 equalization preset value for end port. ・0～10 (Default：7)
PEG Sample Calibrate	Set PEG sample calibrate. ・Disabled ・Enabled ・Auto (Default)
PEG Gen3 Equalization Phase2	Implementation of PEG Gen3 equalization Phase2. ・Disabled (Default) ・Enabled

8.2.8.2. PCI Express Port 1 Configuration (PCIe/PCI-Bridge)

Table 17. PCI Express Port 1 Configuration (PCIe/PCI-Bridge) Setting

Setting	Contents
PCI Express Port 1	Set PCI Express Root Port. When disable Port1, PCI will be also disabled since PCI is connected from Port1. ・Disabled ・Enabled (Default)
PCIe Speed *14	Set PCI Express link speed. ・Auto ・Gen1 (Default) ・Gen2
ASPM *14	Set PCI Express ASPM (Active State Power Management). ・Disabled (Default) ・L0s ・L1 ・L0s and L1 ・Auto
Hot Plug *14	Set hot plug of PCI Express. ・Disabled (Default) ・Enabled
Completion Timeout *14	Set PCI Express Completion Time out. ・default (Default) ・16_55ms ・65_210ms ・260_900ms ・1_3P5s
PME Interrupt *14	Set PME interrupt of PCI Express. ・Disabled (Default) ・Enabled
PME SCI *14	Set PME SCI of PCI Express. ・Disabled ・Enabled (Default)

*14: possible to set by changing PCI Express Port 1 to “Enable”

8.2.8.3. PCI Express Port 3～5 Configuration

Table 18. PCI Express Port 3～5 Configuration Setting

Setting	Contents
PCI Express Port 3～5	Set PCI Express Root Port. ・Disabled ・Enabled (Default)

8.2.8.4. SB USB Configuration

Table 19. SB USB Configuration Setting

Setting	Contents
EHCI1	Set USB ECHI (USB2.0). ・Disabled ・Enabled (Default)
EHCI2	Set USB ECHI (USB2.0) function. ・Disabled ・Enabled (Default)
USB Per-Port Disable Control	Set USB per-Port (#0-5, #8, #9) Disable. ・Disabled (Default) ・Enabled
xHCI Pre-Boot Driver	Set xHCI Pre-Boot router support. ・Disabled ・Enabled (Default)
xHCI Mode	Set xHCI controller run mode. ・Disabled ・Enabled ・Auto ・Smart Auto (Default)
HS Port #1～4 Switchable	Enable switch HS (High Speed) port with xHCI and EHCI. Port is allocated to EHCI by select Disabled. Corresponding SS port is enabled by allocating HS port to xHCI. ・Disabled ・Enabled (Default)

8.2.8.5. SB Serial IRQ Config

Table 20. SB Serial IRQ Configuration Setting

Setting	Contents
Serial IRQ Mode	Set serial IRQ mode. Serial IRQ is active in quiet mode only when needed, while always active in continuous mode. ・Quiet ・Continuous (Default)
Start Frame	Set initial start frame of serial IRQ. ・4 Frames ・6 Frames ・8 Frames

8.2.9. Network Configuration

Table 21. Network Configuration Setting

Setting	Contents
PCH Internal LAN	Set PCH internal LAN. ・Disabled ・Enabled (Default)
LAN OPROM Selection *15	Set PCH internal LAN used for minimum configuration of Quiet Boot. ・Disabled ・Enabled (Default)
Wake on PCH LAN *15	Set wake on PCH LAN. ・Disabled ・Enabled (Default)
ASF Support *15	Set alert specification form. ・Disabled ・Enabled (Default)

*15: possible to set by changing PCH Internal LAN to “Enable”

8.2.10. LPC Configuration

Table 22. L LPC Configuration Setting

Setting	Contents
Onboard UART1	Onboard UART1 address control. ・Disabled ・Enabled (Default)
UART1 Base Address *16	UART1 base address control. ・3F8(Default) ・2F8 ・3E8 ・2E8
UART1 IRQ *16	UART1 interrupt control. ・IRQ 3 ・IRQ 4(Default)
Onboard CIR(UART2)	Onboard CIR address control. ・Disabled ・Enabled (Default)
UART2 Base Address *17	UART2 base address control. ・3F8 ・2F8(Default) ・3E8 ・2E8
UART2 IRQ *17	UART2 interrupt control. ・IRQ 3(Default) ・IRQ 4

*16: possible to set by changing Onboard UART1 to “Enable”

*17: possible to set by changing Onboard CIR (UART2) to “Enable”

8.2.11. SMBIOS Event Log

Table 44. SMBIOS Event Log Setting

Setting	Contents
Event Log	Enable/disable of event log. ・Disabled ・Enabled (Default)
View SMBIOS event log	Display of SMBIOS event log. ・Displays log with “Enter”
Mark SMBIOS events as read	Marking SMBIOS event as read. Marked SMBIOS event is not displayed.
Clears SMBIOS events	Clearing SMBIOS event.

8.2.12. ME Configuration

Table 45. ME Configuration Setting

Setting	Contents
Intel(R) ME	Enable Intel(R) Management Engine. Enabling/disabling of event log. ・Disabled ・Enabled (Default)
ME FW Downgrade	Enable ME FW downgrade. ・Disabled (Default) ・Enabled
ME Debug Event Service	Enable ME debag event service. ・Disabled (Default) ・Enabled
MDES for BIOS	Enable ME debag event service for BIOS. ・Disabled (Default) ・Enabled
ME IFR Features	Set Intel(R) ME Independent firm recovery. ・Disabled ・Enabled (Default)

8.2.13. Thermal Configuration

Table 46. Thermal Configuration Setting

Setting	Contents
Platform Thermal Configuration	・Automatic Thermal Reporting ・Active Trip Point Hi Fan ・Active Trip Point Lo Fan ・Passive TC1 Value ・Passive TC2 Value ・Passive TSP Value ・PCH Thermal Device ・Thermal Sensor Device Enable ・PCH Temp Read Enable ・CPU Energy Read Enable ・CPU Temp Read Enable ・CPU2 Temp Read Enable ・TS On Dimm Enable ・Alert Enable Lock ・ME SMBus Thermal Reporting
Automatic Thermal Reporting	Automatically sets _CRT 、_PSV 、_AC0 based on recommended value of BMG “Thermal Reporting for Thermal Management settings” ・Disabled ・Enabled (Default)
Critical Trip Point *18	Set temperature of ACPI critical trip point (point that OS shuts off system. Note: Target value (POR) with all Intel(R) mobile processors is 100 degrees C. ・POR (Default) / 15℃ / 23℃ / 31℃ / 39℃ / 47℃ / 55℃ / 63℃ / 71℃ / 79℃ / 87℃ / 95℃ / 103℃ / 111℃ / 119℃
Active Trip Point Hi Fan	Set temperature of active trip point hi fan (point that OS increases the processor rotation frequency). ・Disabled / 15℃ / 23℃ / 31℃ / 39℃ / 47℃ / 55℃ / 63℃ / 71℃(Default) / 79℃ / 87℃ / 95℃ / 103℃ / 111℃ / 119℃
Active Trip Point Lo Fan	Set temperature of active trip point lo fan (point that OS decreases the processor rotation frequency). ・Disabled / 15℃ / 23℃ / 31℃ / 39℃ / 47℃ / 55℃(Default) / 63℃ / 71℃/ 79℃ / 87℃ / 95℃ / 103℃ / 111℃ / 119℃
Passive TC1 Value	Set TC1 value to ACPI passive cooling equation. Value is changed by using “+” and ”-“ key. ・Preset value：1～16 ・Default：1
Passive TC2 Value	Set TC2 value to ACPI passive cooling equation. Value is changed by using “+” and ”-“ key. ・Preset value：1～16 ・Default：5
Passive TSP Value	Set TSP value to ACPI passive cooling equation. When passive cooling is enabled, be able to set monitoring frequency to read from OS by 1/10 second. Value is changed by using “+” and ”-“ key. ・Preset value：2～32(Only even number) ・Default：10
Thermal Sensor Device Enable	Set thermal sensor device. Set TSP value to ACPI passive cooling equation. ・Disabled ・Enabled (Default)

*18: possible to set by changing Automatic Thermal Reporting to “Disable”

Setting	Contents
PCH Temp Read Enable *19	Set PCH temperature read. ・Disabled ・Enabled (Default)
PCH Temp Read Enable *19	Set PCH temperature read. ・Disabled ・Enabled (Default)
CPU Energy Read Enable *19	Set CPU energy read. ・Disabled ・Enabled (Default)
CPU Temp Read Enable *19	Set CPU temperature read. ・Disabled ・Enabled (Default)
CPU2 Temp Read Enable *19	Set CPU 2 temperature read. ・Disabled ・Enabled (Default)
TS On DIMM Enable *19	Set DIMM temperature read. ・Disabled (Default) ・Enabled
Alert Enable Lock *19	Set lock all alert activation. ・Disabled (Default) ・Enabled
ME SMBus Thermal Reporting	Set SMBus thermal reporting. ・Disabled (Default) ・Enabled

*19: possible to set by changing Thermal Sensor Device Enable to “Enable”

8.2.14. ICC Configuration

8.2.14.1. DIV-2S

A setup of the clock for BCLK, DMI, PEG, PCIe, PCI33, SATA, and USB3.

Table 47. DIV-2S Setting

Setting	Contents
New frequency[10KHz]	Set frequency in unit of 10KHz.The frequency value will be rounded automatically to closest valid value. Accepted range is limited by maximum/minimum frequency. The change is not applicable until “Apply setting” is executed. ・Preset value：3850(3.85KHz)～40000(40KHz) ・Default：10000(10KHz)
New SSC mode	Spread spectrum clock mode. Set how to spread spectrum from base clock. The change is not applicable until “Apply setting” is executed. ・Up ・Center ・Down (Default)
New SSC spread percent[0.01%]	Set clock spread spectrum at 0.01%.Set spectrum deviation from base clock. Possible range is limited at max supported SSC%. The change is not applicable until “Apply setting” is executed. ・Preset value：0～50(0.5%) ・Default：0

8.2.15. Intel Rapid Start Technology

Table 48. Intel Rapid Start Technology Setting

Setting	Contents
iRST Support	Set iRST. ・Disabled (Default) ・Enabled
Entry on S3 RTC wake *20	Entry on S3 RTC wake. ・Disabled ・Enabled (Default)
Entry after *20	Enabling RTC boot timer when enter to S3. ・Immediately / 1minute / 2minutes / 5minutes / 10minutes(Default) / 15minutes / 30minutes / 1hour / 2hours
Enter S3 on Critical Battery threshold Threshold *20	Enable iRTS when critical battery event occur during S3. ・Disabled ・Enabled (Default)
iRST PARTITION STATUS *20	Set critical battery threshold value of iRST. ・Preset value：1～100 ・Default：15

*20: possible to set by changing Onboard CIR (UART2) to “Enable”

8.3. Security Menu

Table 49. Security Menu Setting

Setting	Contents
Set Supervisor Password	Set or clearing supervisor account password.
Supervisor Hint String	Feeding supervisor hint string with enter key.
Min. password length	Set password with 1-20 characters.

8.4. Boot Menu

Refer Table 50 about Boot priority order.

Table 50. Boot Menu Setting

Setting	Contents
Boot Priority Order	Selection Boot priority setting procedure. The default is as follows: 1.USB HDD 2.USB CD 3.USB FDD 4.ATAPI CD 5.ATA HDD0 6.ATA HDD1 7.ATA HDD2 8.ATA HDD3 9.Other HDD 10.PCI LAN: IBA GE Slot 00CB v1360 11.Internal Shell

8.5. Exit Menu

Table 51. Exit Menu Setting

Setting	Contents
Exit Saving Changes	Exits the setup menu with saving all the changes same as F10, then resets the system automatically.
Exit Discarding Changes	Exits the setup menu without saving the change same as Esc, then resets the system automatically.
Load Setup Defaults	Loads the setup default value same as F9.
Load Optimized Defaults	Loads optimized defaults by boot time and system performance.

Eurotech Worldwide Presence

AMERICAS

USA

DYNATEM
Tel. +1 949.855.3235
Fax +1 949.770.3481
E-mail: sales@dynatem.com
E-mail: tech@dynatem.com
Web: www.dynatem.com

EUROTECH
Toll free +1 888.941.2224
Tel. +1 301.490.4007
Fax +1 301.490.4582
E-mail: sales.us@eurotech.com
E-mail: support.us@eurotech.com
Web: www.eurotech-inc.com

EUROPE

Italy

EUROTECH
Tel. +39 0433.485.411
Fax +39 0433.485.499
E-mail: sales.it@eurotech.com
E-mail: support.it@eurotech.com
Web: www.eurotech.com

To find your nearest contact refer to: www.eurotech.com/contacts

United Kingdom

EUROTECH
Tel. +44 (0) 1223.403410
Fax +44 (0) 1223.410457
E-mail: sales.uk@eurotech.com
E-mail: support.uk@eurotech.com
Web: www.eurotech.com

France

EUROTECH
Tel. +33 04.72.89.00.90
Fax +33 04.78.70.08.24
E-mail: sales.fr@eurotech.com
E-mail: support.fr@eurotech.com
Web: www.eurotech.com

Finland

EUROTECH
Tel. +358 9.477.888.0
Fax +358 9.477.888.99
E-mail: sales.fi@eurotech.com
E-mail: support.fi@eurotech.com
Web: www.eurotech.com

ASIA

Japan

ADVANET
Tel. +81 86.245.2861
Fax +81 86.245.2860
E-mail: sales@advanet.jp
E-mail: tsupport@advanet.jp
Web: www.advanet.co.jp

India

EUROTECH
Tel. +91 80.43.35.71.17
E-mail: sales.in@eurotech.com
E-mail: support.in@eurotech.com
Web: www.eurotech.com

EUROTECH

www.eurotech.com

EUROTECH HEADQUARTERS
Via Fratelli Solari 3/a
33020 Amaro (Udine) – ITALY
Phone: +39 0433.485.411
Fax: +39 0433.485.499

For full contact details go to: www.eurotech.com/contacts